REMARKS

This application was filed with 12 claims. Claims 1-12 have been rejected. Claims 1, 2, 5, and 10-12 have been amended. Therefore, Claims 1-12 are pending in the Application. Reconsideration of the application based on the remaining claims as amended and arguments submitted below is respectfully requested.

Amendments to Drawings

The Examiner has objected to the drawings. Applicant is submitting with this response a set of proposed new drawing Figures 1-5. Note that for purposes of enlarging the contents of Fig. 5, the proposed new drawings include two drawing sheets for Fig. 5, labeled Fig. 5A and Fig. 5B.

Claim Rejections - 35 U.S.C. § 102(b)

Claims 1, 2, 4-6, and 8-12 have been rejected under 35 U.S.C. § 102(b) as being anticipated by Choi, U.S. Patent No. 6,201,832. In response, Applicant has amended Claims 1, 2, 5, and 10-12.

Applicant's invention includes a timing equalizer filter prior to the timing loop function to improve its performance in the presence of loop distortion. This timing equalizer is decoupled from the primary linear equalizer in the receiver, thus removing the conflict commonly found between the equalizer and the timing loop when both are adapting to adjust timing.

Choi teaches that the output from the system equalizer channel (200 on Fig. 2) is fed to the timing loop (See line L495 connected from the output of the loop filter 80 to the interpolation filter 20). Thus, Choi has a single path from the A/D

converter 16 through the equalizer to the timing loop. Applicant's invention, by comparison, teaches two separate data paths (see Fig. 5A). One of the paths is similar to Choi except that it does not contain the timing loop. The other path has many of the circuits Choi teaches and contains the timing loop. Furthermore, whereas Choi updates the equalizer and the timing loop in the same path, Applicant's invention teaches that the timing loop path not contain an adaptive equalizer, and thus there is no timing phase conflict between the equalizer and the timing loop in the present invention.

Claim 1 as amended makes it clear that the timing equalizer is functionally independent from the linear equalizer, whereas in Choi, this is not the case.

Claim 2 has been amended to clarify that the timing equalizer coefficients, in one embodiment, are derived from the linear equalizer coefficients, as opposed to being continuously updated with the linear equalizer coefficients. Choi teaches that timing equalizer and timing loop are in the same path.

Therefore, Claims 1and 2 as amended are not anticipated by Choi. Claim 4 is dependent on Claim 1 and therefore should be allowable as well.

Claim 5 has been amended to include the step that the timing equalizer filter is operated in a data path separate from the linear equalizer. As seen on Fig. 2, Choi discloses a common data path for the "interpolation filter 20" and the adaptive equalizer channel 200, such that the output from loop filter 80 is provided as an input to interpolation filter 20 as well as to block 160. Applicant's Fig. 5A shows that the timing equalizer filter of the present invention has an independent data

path. Claim 6 is dependent on Claim 5. Therefore, Claims 5 and 6 are not anticipated by Choi.

Claim 8 includes the step of positioning the timing equalizer filter such that operation of the timing loop can proceed independently of subsequent adjustment of the linear equalizer. Choi does not disclose this step because as shown in Fig. 2, the timing loop and linear equalizer channel are in the same data path. Therefore, Claim 8 and Claim 9 (which is dependent on Claim 8) are not anticipated by Choi.

Claims 10, 11, and 12 each have been amended to clarify that the timing equalizer filter is functionally independent from the linear equalizer. Choi does not teach this feature because the interpolation filter and adaptive timing equalizer channel 200 are in the same data path. Therefore, Claims 10-12 should be allowable over Choi.

For the foregoing reasons, the rejection of Claims 1, 2, 4-6, and 8-12 under 35 U.S.C. § 102(b) should be withdrawn.

Claim Rejections - 35 U.S.C. § 103

Claims 3 and 7 have been rejected under 35 U.S.C. § 103(a) as being unpatentable over Choi in view of Cheng et al., U.S. Patent No. 5,818,378.

Claim 3 is dependent on Claim 1 which, as discussed above, provides that the timing equalizer filter is functionally independent from the linear equalizer. Choi teaches away from this important characteristic of the present invention by providing a common data path for the interpolation filter 20 and adaptive equalizer channel 200. Cheng does not teach this feature either. In addition, Claim 3 specifies that the

timing equalizer is provided with pre-determined coefficients based on a loop of moderate length. These are compromise coefficients based on a moderate length loop that are suitable for a wide variety of cable lengths. Cheng discloses an active cable estimation circuit. The purpose of this cable length estimation circuit is measure the loop length to facilitate compensation for distortion. Applicant's invention is quite different in that the compromise coefficients are "pre-determined" and supplied to the timing equalizer filter for ongoing use. There is no active determination or updating of these compromise coefficients as taught by Cheng and Choi in combination. Claim 7 is similar in that it is dependent on Claim 5 which provides for separate data paths, a feature not taught by either Choi or Cheng. Therefore, Claims 3 and 7 should be allowable.

Applicant has commented on some of the distinctions between the cited references and the claims to facilitate a better understanding of the present invention. This discussion is not exhaustive of the facets of the invention, and Applicant hereby reserves the right to present additional distinctions as appropriate. Furthermore, while these remarks may employ shortened, more specific, or variant descriptions of some of the claim language, Applicant respectfully notes that these remarks are not to be used to create implied limitations in the claims and only the actual wording of the claims should be considered against these references.

Pursuant to 37 C.F.R. § 1.136(a), Applicant petitions the Commissioner to extend the time for responding to the December 18, 2003, Office Action for 3 months from March 18, 2004, to June 18, 2004. Applicant encloses herewith a check in the

amount of $950 made payable to the Director of the USPTO for the petition fee. The Commissioner is authorized to charge any deficiency or credit any overpayment associated with the filing of this Response to Deposit Account 23-0035.

Respectfully submitted,

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ATTORNEY FOR APPLICANT

CERTIFICATE OF FIRST CLASS MAILING

I hereby certify that this Response and Amendment, including new drawing Figures 1-5 and an extension fee check in the amount of $950, are being deposited with the United States Postal Service as first class mail in an envelope addressed to:

Mail Stop Amendment
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

on June 18, 2004.

Mark J. Patterson

Signature
Registration Number 30,412

6/18/2004

Date